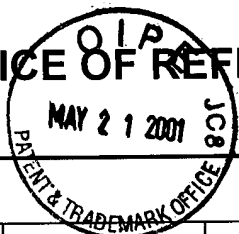


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APPLICANT(S) Jerrold L. King et al.

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*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
✓	A	5,519,251	5/21/96	Sato et al.	257	666	
	B	5,442,233	8/15/95	Anjoh et al.	257	675	
	C	5,136,366	8/4/92	Worp et al.	357	72	
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	F	5,397,921	3/14/95	Karnezos	257	779	
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✓	R	Shinko Technology Update, Dec. 12, 1994, p. 141.
	S	"Mitsubishi scales down IC package," Electronic Engineering Times, Aug. 22, 1994, p. 13.
	T	TA 8.2: A 34 ns 256 Mb DRAM with Boosted Sense-Ground Scheme, 1994 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 140-141.

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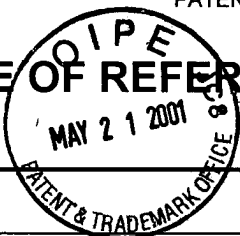
\* A copy of this reference is not being furnished with this office action  
See Manual of Patent Examining Procedure, section 707.05(a)

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